# A Silicon Surface Code Architecture Resilient Against Leakage Errors

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Spin qubits in silicon quantum dots are one of the most promising building blocks for large scale quantum computers thanks to their high qubit density and compatibility with the existing semiconductor technologies. High- delity gates exceeding the threshold of error correction codes like the surface code have been demonstrated. However, there are other types of error | such as charge leakage and propagation | that may occur in quantum dot arrays and which cannot be corrected by quantum error correction codes, making them potentially damaging even when their probability is small. We propose a surface code architecture for silicon quantum dot spin qubits that is robust against leakage errors by incorporating multi-electron mediator dots. Charge leakage in the qubit dots is transferred to the mediator dots via charge relaxation processes and then removed using charge reservoirs attached to the mediators. A stabiliser-check cycle, optimised for our hardware, then removes the correlations between the residual physical errors. Through simulations we obtain the surface code threshold for the leakage errors and show that in our architecture the damage due to leakage errors is reduced to a similar level to that of the usual depolarising gate noise. Our use of an elongated mediator dots creates spaces throughout the quantum dot array for charge reservoirs, measuring devices and control gates, providing the scalability in the design.

## I. INTRODUCTION

Universal quantum computers promise speed-up in crucial areas like simulation of materials and molecules [1], search [2, 3] and sampling [4, 5], yet they require precise control of error-free quantum states. Quantum error correction codes allow us to trade gubit number for precision in controlling quantum states, with the surface code being particularly attractive due to its 2D structure, local checking operations and high error threshold close to 1%. Surface code architectures have been proposed for leading quantum information processing platforms including superconducting gubits [6]. trapped ions [7] and semiconductor spin qubits [8, 9]. However, the qubit overheads can be signi cant: it is estimated that > 2 10<sup>8</sup> physical qubits with gate error rate 10<sup>-3</sup> might be needed to perform a non-trivial Shor's factoring algorithm using surface codes [10]. These considerations motivate the development of qubit implementations which o er the prospect for high-density 2D arrays. The high-qubit density o ered by silicon-based spin (SS) qubits (as high as  $10^9$  cm<sup>-2</sup>) combined with the possibility of leveraging the conventional semiconductor integrated circuit industry [11] make this platform attractive for fault-tolerant universal quantum computing.

Like all qubit hardware approaches, scaling up SS qubits brings a number of practical requirements associated with qubit addressing for calibration, tuning, operation and readout. Indeed, the high qubit densities o ered

by SS gubits leads to challenges in routing classical control lines, while minimising cross-talk and managing heat dissipation [11]. A number of architectures for scaling up SS gubit arrays have been proposed to address such challenges: for example, Veldhorst et al. [12] proposed a compact quantum dot array controlled via a crossbar geometry, enabling N qubits to be controlled with  $\sqrt{N}$  classical control lines, albeit using control transistors below the dimensions of current technology [11]. Li et al. [13] went further with a half- lled crossbar architecture that provides more space for classical control lines, though the use of shared control lines brings tight requirements for qubit homogeneity and limitations on the parallelisability of operations. Buonacorsi et al. [14] have suggested connecting many small quantum dot modules using electron shuttling in order to provide the space for individual control lines. Smaller quantum dot modules are also easier to calibrate and the operations within the modules

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bated) by the usual quantum error correction protocols, they will accumulate and eventually corrupt the surface code even if the probability of these leakage errors is very small. Furthermore, unlike most of the other types of leakage errors [15{20] which occur as independent events, a leaked charge from one dot might propagate through the quantum dot surface code array and corrupt other dots. Charge leakage errors thus could be very damaging to the surface code due to the correlations in errors.

In this Article, we introduce a surface code architecture based on SS qubits that is designed to be robust against leakage errors. We rst introduce the components of our hardware in Section II, and then discuss leakage errors in our architecture in Section III. Then, in Section IV, we describe how surface code stabiliser checks are performed, and obtain a threshold for the gate errors and leakage errors. Finally, we summarise the key features of this approach and discuss possible improvements and extensions.

# II. PHYSICAL IMPLEMENTATION

The physical layout of the silicon quantum dot surface



FIG. 2. Core two-qubit gate between data and ancilla qubits, achieved via a mediator. Three quantum dots with orbital L=R in the left/right dot, each of which is either a data dot or one half of an ancilla structure, and orbitals 1 and 2 in the middle mediator dot. We consider a total of four electrons in this three-dot system and assume the charging energy of the side dots is su ciently large (due to their small size) to forbid further occupancy. Electrons may be excited to the mediator state 2 from any of L, R or 1 orbitals, with some energy cost indicated.

would yield in J. To push into the J regime, the platform could be further engineered for larger J values, or for the reduction in disorder levels giving rise to variation of electron g-factors such that they can be mitigated e ectively using the Stark shift.

#### E. Charge Reservoirs and Initialisation

Charge reservoirs remain an integral component of modern test-bench quantum devices as they are used to supply electrons to quantum dots, facilitate traditional spin-to-charge readout [61] or more recent improved methods [62, 63], as well as providing a relaxation path for rapid spin initialisation [47]. However, modern concepts of scaled qubit platforms that exploit CMOS technology typically envisage larger devices with densely-packed quantum dots, leading to reservoirs being pushed to the borders of large 1D [29] or 2D [12] arrays. Other architectures have the capacity for reservoirs to be located in specialised modules where spins could then be shuttled into arrays through the use of long-distance highways [13]. With the relative absence of reservoirs in many modern architectures, spin initialisation and readout relies predominantly on Pauli spin blockade methods, with some schemes also utilising thermal relaxation as an initialisation method [11].

In the architecture presented here, we strive to maintain the advantages of having integrated spin reservoirs, without compromising the advantages of CMOS as a platform capable of realising arrays of densely-packed gubits. This is achieved through the spatial separation a orded by the larger scale mediator dot between each data/ancilla dot as seen in Figure 1. With a gate pitch of 30{40 nm [23, 34] in recent 2D planar SiMOS QD designs, and with the possibility of reducing this through the use of smaller length scales (e.g. more recent CMOS technology nodes), the indicated 300 nm separation due to the mediator generates enough space for the integration of the reservoirs as well as the planar fan-out of metallic gate structures required to de ne/con ne the 2D quantum dot structures. Speci cally, this facilitates the ability to maintain gated connections between the reservoir and the mediator dot, meaning the tunnel rate can be tuned or made switchable for either rapid interaction as required during initial population of a qubit array, or appropriately tuned for slow reset of mediator dots during periods of inactivity.

The smallest energy scale for the mediator system is  $_{M}$  10 GHz, which remains 5 larger than con-

qubits in semiconductor quantum dots. Wang *et al.* [70] measured the charge relaxation time in Si/SiGe double quantum dots, showing strong dependence on the tunnelling energy between the orbitals and weak dependence on the detuning between the orbitals. For the tunnelling energy regime that we are interested in  $(t \ 1 \text{ GHz})$ , the relaxation time was around 10 ns, which is much shorter than the other time scales in our systems (all the gates in our system operate at  $\mu$ s time scale). Hence, we can assume that once a leakage error occurs (in which a charge escapes from a qubit dot), a relaxation process quickly takes place, in which an electron in one of the adjacent mediator dots (*not* necessarily the one that our charge escapes to) hops down to II the empty qubit dot. Such a relaxation process restores our qubit dots back into having one e ective electron spin, and thus back into the computational subspace. Therefore, even without any active leakage error detection and correction or applications of any leakage reduction protocols, our architecture has a useful inherent behaviour whereby charge de cit transfers from gubit dots to mediator dots.

The relaxation process that restores the charges in the qubit dots can, however, result in missing/extra charges in the mediator dots, which, uncorrected, would produce faulty exchange gates. This can be corrected by connecting all the mediators to the charge reservoirs that are used for the initial population of the quantum dot array. Since the mediators do not carry any quantum information, such connection to reservoirs should not introduce qubit errors.

Errors due to unwanted coupling between the charge reservoirs and the qubit array are minimised by decreasing the tunnelling energy between the reservoir and the mediators, though this produces a longer reset time for the mediators. As we will see in Section IV, our surface code is partitioned into regions which are active/inactive at di erent times during a full cycle. This provides an opportunity for a given mediator to reset with its nearby reservoir during an idle period, without adding delay to the error correction processes. The tunnel coupling between mediator and reservoir can be minimised to the level required to give a reliable state reset within the execution time of half of a stabiliser check, and thus minimise any charge noise injection into the mediator and rest of the circuit.

Without the use of mediators, leakage errors apply directly to the qubit dots and require leakage correction schemes to be applied. As discussed in Appendix D, such schemes would introduce large qubit/runtime overheads [67, 69], limits on the choice of data/ancilla qubits [68] and/or require extra components for charge detection or reset introduced within a potentially dense qubit array. In contrast, in the architecture we propose here the leakage errors are addressed by resetting the mediators using charge reservoirs. No additional components are needed since the reservoirs are also used for qubit initialisation and no additional runtime is introduced since the mediator resets can be carried out in



FIG. 4. Ordering of stabiliser check cycles. Each plaquette is given one of four colours, such that plaquettes of the same colour share no data qubits between them. Stabiliser checks of all plaquettes of a given colour are carried out simultaneously, in the sequence indicated by the arrows.

rotations can be implemented as a combination of X and Y rotations (which can be slow as noted in Section II D), or using the Stark shift whose speed is limited by the detuning range and whose accuracy relies on careful calibration. Fortunately, in our stabiliser-check circuit, most of the Z rotations on the data qubits can be implemented in a virtual way by shifting the phases of all the future single-qubit rotations pulses [78], and the Z rotations on the ancillae can be omitted since we are performing symmetric operations on the singlet subspace (see Appendix A4



FIG. 5. Surface code two-qubit gate error threshold calculations in the case of no leakage error ( $p_{\text{leak}} = 0$ ) assuming (a) *S* gates with error rate  $p_2$  or (b)  $\frac{p_1}{\text{SWAP}}$  gates with error rate  $p_2=2$ . In all calculations, the error rate of single-qubit gates ( $p_1$ ) and two qubit gates ( $p_2$ ) is assumed to be xed  $\frac{p_1}{p}$ 



FIG<sub>p</sub>6. Surface code leakage error  $p_{\text{leak}}$  threshold calculations assuming the use of (a) *S*-gates with error probability  $p_2 = 0.5\%$ , (b) SWAP gates with error rate  $p_2 = 2 = 0.25\%$ , or (c) perfect gates ( $p_2 = 0$ ). In all calculations, the error rate of single-qubit gates ( $p_1$ ) and two qubit gates ( $p_2$ ) is assumed to be xed  $\frac{p_1}{p_2} = 0.1$ . *d* is the code distance of the surface code.

coherence time of spins in silicon measured in devices to date can be tolerated by our surface code architecture.

## V. CONCLUSIONS AND OUTLOOK

We have introduced a surface code architecture implemented using spin qubits in silicon quantum dots that is robust against leakage errors through its use of multielectron mediator dots. Our approach e ciently uni es the task of maintaining a proper charge distribution (essential for any SS quantum device) together with the task of performing the stabiliser cycles required by the surface code. Charge leakage from the qubit dots is transferred to the mediator dots via fast charge relaxation, and removed using charge reservoirs attached to the mediators, reducing the leakage errors to the level of standard computational errors that can be corrected by the surface code. We nd that our stabiliser check cycle removes time and space correlations in the remaining computational errors, which can be highly damaging to surface codes. The depth of the stabiliser-check circuit was reduced by the symmetry of the double-dot ancillae and virtual Z gates. Through simulations, we nd that the surface code threshold for the computational errors arising from leakage errors is 0.66% in the absence of gate errors, showing that its e ect can be limited to that of standard depolarising gate errors. Under a reasonable

## Appendix A: Two ways to achieve CZ between data and ancilla qubits

#### 1. Hamiltonian

The two-spin Hamiltonian is ex

 $H = \frac{1}{2} \underbrace{(E_1 Z_1 + E_2 Z_2)}_{H_0: \text{ Zeeman}} + \underbrace{\frac{J}{2} \text{SWAP}}_{H_{ex}: \text{ exchange}}$ (A1) splitting interactions

The Zeeman splitting  $H_0$  can be further split into:

$$\frac{\frac{1}{2}(E_1Z_1 + E_2Z_2)}{H_0: \text{ Zeeman}} = \frac{\frac{E_z}{2}(Z_1 + Z_2)}{H_z: \text{ average}} + \frac{\frac{1}{2}(Z_1 - Z_2)}{H : \text{ Zeeman}}$$
splitting Zeeman splitting splitting gradient

where  $E_{Z} = \frac{E_{1} + E_{2}}{2}$ ,  $= \frac{E_{1} - E_{2}}{2}$ .

## 2. *J*: simple exchange interaction

Since J, and  $[H_{ex}; H_Z] = [SWAP; Z_1 + Z_2] = 0$ ,  $H_{ex}: I = e^{iH_0t}H_{ex}e^{-iH_0t} = H_{ex}$ 

i.e. to perform the exchange interaction in the rotating frame is just the same as performing the exchange interaction in the lab frame.

The evolution operator due to  $H_{ex}$  is given by:

$$U_{ex}(t) = e^{-iH_{ex}t} = e^{-iSWAP\frac{Jt}{2}}$$

A SWAP gate corresponds to  $\frac{Jt}{2} = \frac{1}{2}$ , and a  $\frac{p_{\overline{p}WAP}}{p_{\overline{p}WAP}}$ 

have di erent forms in the shifted rotating frame and might not be achievable through our Hamiltonian.

Following such arguments, we nd that for the CZ gate constructed using the exchange-interaction, the Z bracketed by the two ' SWAPs cannot be applied in a virtual way, while the two Z rotations outside the ' SWAPs can. For the dipole-dipole CZ gate, all the Z rotations can be applied in a virtual way.

However, there is another caveat. For the virtual Zrotation to work, we need to do the measurements in Z basis at the end, so that all the remnant Z rotation for compensating for the virtual Z gates will have no effect on the measurements (though we can use the shifted one qubit gate to change the measurement basis). Our ancilla measurement does not use a standard basis: our measurement only tells us whether the ancilla is in the singlet or triplet state, where the singlet state and the triplet states does not corresponds to a qubit representation. Thus, we cannot use virtual Z gates here for our ancilla qubits, but can instead permute all the Z rotations (besides the one bracketed by SWAP) to the position right after the initialisation of the singlet state. We then use the fact that the initial singlet state is invariant under symmetric gates operating on both ancilla dots, to see that there is no need to apply the Z rotations at the ancilla (besides the one bracketed by  $^{\prime}$  SWAP).

Hence, under either approach to implement a CZ gate, the only single-qubit, gate that we need to implement is the Z bracketed by SWAPs. All the other Z rotations can be either implemented in a virtual way or can be omitted due to the property of our ancilla qubits.

#### 5. Comparison of the two implementations of CZ

#### a. Operation time

We denote the characteristic time scale of exchange interaction as  $T_J = J$ , and that of Z gate as  $T_Z$ . The time we needed to achieve a CZ using dipole-dipole like interaction is just  $T_J$ , no single-qubit gates needed. On the other hand, the time we need to achieve a CZ using exchange interaction is  $T_J + T_Z$ . The extra term here is due to the Z gate that we need to explicitly implement.

#### b. Errors

## Errors due to uctuation of Jt:

The ideal exchange phase for  $P_{\overline{SWAP}}$  is  $_{sw} = Jt_{sw} = \frac{1}{2}$ . We will denote the variance in  $_{sw}$  due to uctuations in exchange strength J or operation time t rota33(q.)]TJ -191.6495 Td 382 Tg [(T 3820 -11.457 Td [(39c)2)cill(v)55(a 382372(p)

However, over- and under-rotations of occur in the experiment due to imprecise pulse timing t or uctuation of interaction strength E. If there is a 50% percent chance of over and under rotation by 1, we have:

$$U( ) = e^{i( )h}$$

$$e^{i h} I i h \frac{2}{2}h^{2}$$

$$= U( ) I \frac{2}{2}h^{2} i h$$

Then the e ective operation is just

$$U_{j}() = \frac{1}{2}U(+) U^{y}(+) + \frac{1}{2}U(-) U^{y}(-)$$
$$= I - \frac{2}{2}h^{2} U(-) U^{y}(-) I - \frac{2}{2}h^{2} + {}^{2}hU(-) U^{y}(-)h$$
(B3)

Similar channels are obtained for other symmetric over/under-rotation distributions that are centred on the correct rotation angles.

## a. h is unitary

If h is unitary (and remember it is also Hermitian since it is the normalised Hamiltonian), e.g. h is SWAP or Pauli, then (B3) turns into

$$U_{y}() = 1 \quad {}^{2} \quad U() \quad U^{y}() + {}^{2}hU() \quad U^{y}()h \quad (B4)$$

i.e. we have either perfect U() or  $^2$  probability of having a h error on top of  $U_{ex}()$ .

## b. Twirling

Twirling is a technique use for transforming the given

hence the CZ gate) can be turned on and o by shifting the detuning of the mediator dot with respect to the side dots to switch L=R between on and o

and a small o diagonal (tunnelling) part  $rH^{(1)}$ .

$$rH^{(1)} = \begin{matrix} O & 0 & 0 & 0^{1} & jTi = & 0^{(0)} \\ B0 & 0 & t+t & 0C & jSi = & 1^{(0)} \\ 0 & t+t & 0 & 0^{A} & jion_{+}i = & 2^{(0)} \\ 0 & 0 & 0 & 0 & jion_{-}i = & 3^{(0)} \end{matrix}$$

r here is the ratio between the o -diagonal tunnelling energy t and the diagonal detuning energy :

$$r = \frac{t}{2}$$
 1:

Here we see that  $rH^{(1)}$  only mixes jSi and  $jion_+i$  and leaves jTi and  $jion_+i$  unchanged.

Starting from the eigenstates and the eigenenergies of  $H^{(0)}$ , we can obtain the eigenstates and the eigenenergies of H using perturbation theory:

$$H = H^{(0)} + rH^{(1)}$$
  

$$jni = n^{(0)} + r n^{(1)} + r^2 n^{(2)} +$$
  

$$E_n = E_n^{(0)} + rE_n^{(1)} + r^2 E_n^{(2)} +$$

the superscript (m) denotes the  $m^{\text{th}}$ -order correction.

## b. Perturbation theory

• Change in states ) leakage error:

$$r \ 1^{(1)}{}^{E} = \frac{X}{E_{n}^{(0)} \epsilon E_{1}^{(0)}} n^{(0)}{}^{E} \frac{n^{(0)} r H^{(1)} 1^{(0)}}{E_{1}^{(0)} E_{n}^{(0)}}$$

$$= 2^{(0)}{}^{E} \frac{2^{(0)} r H^{(1)} 1^{(0)}}{E_{1}^{(0)} E_{2}^{(0)}}$$

$$= \frac{t + t}{U} 2^{(0)} \qquad (F1)$$

$$r \ 2^{(1)}{}^{E} = \frac{X}{E_{n}^{(0)} \epsilon E_{2}^{(0)}} n^{(0)}{}^{E} \frac{n^{(0)} r H^{(1)} 2^{(0)}}{E_{2}^{(0)} E_{n}^{(0)}}$$

$$= 1^{(0)}{}^{E} \frac{1^{(0)} r H^{(1)} 2^{(0)}}{E_{2}^{(0)} E_{1}^{(0)}}$$

$$= \frac{t + t}{U} 1^{(0)} \qquad (F2)$$

Hence

$$j1i = 1^{(0)} \stackrel{E}{=} \frac{t+t}{U} 2^{(0)} \stackrel{E}{=} j2i = 2^{(0)} \stackrel{E}{=} + \frac{t+t}{U} 1^{(0)} \stackrel{E}{=}$$

• Change in the ground state energy ) exchange interaction:

The leading non-vanishing order of energy shift is

$$r^{2}E_{1}^{(2)} = 2\frac{(t+t)^{2}}{U}$$

$$r^{2}E_{2}^{(2)} = 2\frac{(t+t)^{2}}{U}$$
*c.* Leakage oscillation

Now if we start in the state of  $jSi = 1^{(0)}$  the probability of leaking into  $jion_+ i = 2^{(0)}$  is:

$$D_{2}(0) e^{-i\hat{F}t} 1(0) = X_{2}(0) e^{-i\hat{F}t} 1(0) = X_{2}(0) e^{-i\hat{F}t} 1(0) = E_{2}(0) e^{-iE_{1}t} 2(0) n n 1(0) = E_{2}(0) e^{-iE_{1}t} 2(0) 1 1 1(0) + e^{-iE_{2}t} 2(0) 2 2 1(0) = 1 = \frac{1}{2} + \frac$$

Hence,

$$\overset{D}{2^{(0)}} e^{-i\hat{H}t} 1^{(0)} \overset{E}{=} 4 \frac{t+t}{U} \sin^2 \frac{E_2 E_1}{2} t$$

To the leading order  $E_2$   $E_1 = U$ . Hence, the probability of leaking has the magnitude of  $r^2$  and oscillates with the frequency  $\frac{U}{2}$ 

FIG. 7. The probability of being in a di erent spin/charge states during one period of exchange interaction, following an initial j''; #i state. Note that the green and red lines completely overlap, and both represent a leakage probability. Here we have used  $r = \frac{t}{2} = 0.1$ .

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